

November 18, 2003

To: Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572 28 Davis Avenue Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/649,472 08/27/03

Juing-Yi Cheng, Kevin Su

A NOVEL CHEMICAL-MECHANICAL POLISHING (CMP) PROCESS FOR SHALLOW TRENCH ISOLATION

Grp. Art Unit:

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on November 2), 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Signature/Date

TSMC-00-484B

U.S. Patent 6,043,133 to Jang et al., "Method of Photo AlignOent for Shallow Trench Isolation Chemical-Mechanical Polising," discloses a CMP STI process with reverse mask.

The following four U.S. Patents dislose various STI processes:

- 1) U.S. Patent 6,107,159 to Chuang, "Method for Fabricating a Shallow Trench Isolation Structure."
- 2) U.S. Patent 5,837,612 to Ajuria et al., "Silicon Chemical Mechanical Polish Etch (CMP) Stop for Reduced Trench Fill Erosion and Method for Formation."
- 3) U.S. Patent 5,950,093 to Wei, "Method for Aligning Shallow Trench Isolation."
- 4) U.S. Patent 5,889,335 to Kuroi et al., "Semiconductor Device and Method of Manufacturing the Same."
- U.S. Patent 5,994,201 to Lee, "Method for Manufacturing Shallow Trench Isolation Regions," discloses a method for manufacturing shallow trench isolation regions using a first stop layer and a second stop layer as two polishing stop layers, or a polishing stop layer and an etching stop layer, respectively.

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- U.S. Patent 5,930,645 to Lyons et al., "Shallow Trench Isolation Formation with Reduced Polish Stop Thickness," discloses a method of manufacturing a semiconductor device comprising trench isolation.
- U.S. Patent 6,043,133 to Jang et al., "Method of Photo Alignment for Shallow Trench Isolation Chemical-Mechanical Polishing," discloses a method of removing an shallow trench isolation (STI) oxide layer from over alignment marks.

Sincerely,

Stephen B. Ackerman, Reg. No. 37761

Doctor (Museum (Continus) Form PTO-1449 TSMC-00-484B INFORMATION DISCLOSUFE CITATION Appacant IN AROUPPLEATION Filling Does (Usia several shouts if nocessary) U. S. PATENT DOCUMENTS ALMO DATE REMILLIZE DOCUMENT HUMBER NAME CLASS **NOCUA** DATE 427 40ns 424 438 296 432 438 438 401 257 797 FOREIGN PATENT DOCUMENTS Translation CLASS SUBCLASS COUNTRY DOCUMENT NUMBER OATE 8 YES (Including Author, Tibe, Date, Pertinent Pages, Etc.) OTHER DOCUMENTS EXAMER DATE CONCIDERED

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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant

TSMC-00-484B

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ASSOCIATE POWER OF ATTORNEY

I hereby appoint Rosemary L.S. Pike, registration number 39,332, as my associate attorney in this case. Her telephone number is (765) 453-0866.

Please continue to direct all correspondence in this case to the undersigned attorney.

Respectfully submitted,

Stephen B. Ackerman,

Principal attorney of record